Line Power Extension Method for Capacitor Reduction for AC-DC Application

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***Abstract*— Small size now becomes one of the top valued features for cellphone and laptop power adapter, especially after the USB-PD standard released. Although semiconductors have shrunk the footprint significantly, passive components, especially the electrolytic capacitors, barely reduced their size over the past decade. This paper proposed the line power extension method to reduce the value and size of the high-voltage input capacitor, which occupies up to ¼ of the total converter volume. If same capacitance is desired, the proposed method can reduce the wide voltage gain that is required by the universal AC input. Besides, due to the extended conduction time of the line power, the current stress in the rectifier is also reduced. In a 60 W prototype, 30% of capacitance reduction and 25% of size reduction is achieved as compared to conventional full bridge.**

Keywords — universal; power adapter; SRC; series resonant converter; wide voltage; power delivery; USB PD

I. INTRODUCTION

Technologies associated with the power adapters for laptops and cellphones are fast advancing with the market rapidly growing [1]–[3]. With the new protocols and devices unveiled, the converter design faces new challenges. On one hand, the newest generation of power adapters need to satisfy those stringent requirements of the fast-charging protocols, including universal AC input, high output current, and multiple output voltage levels, *etc* [4]. On the other hand, the products should be designed towards the highest level of efficiency and miniaturization, so to stand out from the competition. Between small size and high performance – the two top-valued features, small size might be of more concern, especially from the consumer's perspective. The reason is that a product with high efficiency might not necessarily be compact, but a compact product must be highly energy efficient, in order to achieve acceptable thermal performance.

To reduce the size, the converters are being improved from various aspects with the advanced technologies and the state-of-art materials.

Firstly, the topologies are evolving. With the advances of semiconductor fabrication, CPUs nowadays consumes less power. Today, adapters' power profile is de-rated to 60 W level without mandatory power factor correction [5]. At this power level, Flyback converter has been the dominant topology since the era of switch-mode power supply, thanks to its simple implementation and low cost. However, further reducing the size will require to increase the switching frequency, then the conventional Flyback struggles to achieve acceptable size and thermal performance due to the significantly increased switching loss. Much frequency and efficiency improvement as the Flyback earns with the active clamp technique [6][7], the cost and complexity increase. On the other hand, resonant converters are well known for their high performance in high frequency and very high frequency (VHF) applications [8]. As compared to Flyback converters, resonant converters have generally lower current stress due to the longer power-transfer time in each switching cycle, easier implementation of soft switching on all switches, and better transformer performance operating in two quadrants. The downside is that the cost is believed to be higher. Besides, the load regulation and operational voltage range are generally weaker for resonant converters. In a nutshell, a technology shift is being seen in this sector from conventional hard-switching converters operating at 65-130 kHz to (quasi-) resonant converters operating at a few hundred kilohertz until megahertz [9].

Secondly, the magnetic materials, e.g. the ferrites, are also being refined for operating at high frequency [10]. The primary motivation to push up the switching frequency is to reduce the size of the passive components, especially the magnetic components. However, the reduction of size will be bottlenecked by the increased core loss due to the higher flux density, as well as the increased winding loss due to the reduced window size [11]. Thus, improving the performance of

the magnetic material at high frequency is essential to further reduce the converter size. It has been reported of the development and release of new materials optimized for megahertz operation and featured significantly reduced core loss per unit volume [12] [13]. Besides, planar transformers with PCB windings are gaining popularity in recent literatures and products [14]. With the windings printed on the board, the height of the magnetic components can be significantly reduced [15]. Moreover, the connection of the windings with other parts can be done on the board directly. Therefore, there is no need to solder the magnetic components, and the AC current loss at the soldering terminal is removed [16]-[18].

Thirdly, the power semiconductors are also getting prepared for the high frequency era. Besides the regular upgrade of silicon MOSFET, wide bandgap devices exemplified by the gallium nitride become commercially available at 650 V rating. Despite the technology is still under development, GaN HEMT is reported to achieve significantly lower output capacitance (Coss) enabling much faster switching transient, with similar conduction resistance (Rdson) to the best-in-class silicon MOSFET. Therefore, the die size of GaN HEMT can be much smaller for given current capability [19]. Besides, the packaging technique is also moving forward, which reduces the parasitics – one of the major obstacle for high frequency operation. New packages of MOSFETs provides source terminal with Kelvin connection that is dedicated for gate driving [20]. This way, the common-source inductor can be eliminated to achieve faster switching transient with less ringings. Further, quite a few manufacturers now provide GaN HEMTs without bonding wires, and some even have the bridges [21] and the driving circuits [22] integrated in the same chip. These emerging packaging techniques are expected to bring about reduced parasitics and faster switching performance all within significantly smaller footprint.

With all these advanced technologies to shrink the footprint and profile of the semiconductors and magnetics, our power adapters today have reduced the size for more than 4 times as compared to years ago. However, examining the inside of the adapters, one cannot lose sight of the electrolytic capacitors, either at the input end for non-PFC applications or at the output end for PFC cases. These capacitors that used for AC power buffering has barely reduced the size since decades ago. In a modern adapter, these capacitors can take up to a quarter of the total volume. Thus, reducing this capacitor value and size can have significant influence on the converter size.

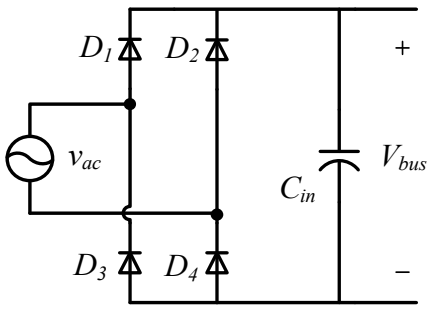


Fig. 1. Conventional full bridge rectifier without PFC

Today, with the development of USB Power Delivery, most power adapters are designed for 15 W-60 W [6]. At such power level, power factor correction is not mandatory [7]. Thus, full bridge plus a buffering capacitor as shown in Fig. 1 is often used to convert the 100-240 VAC input into DC voltage. Such configuration utilize the line power only before its peak value, which is easy to implement but not as desired. This paper focuses on reducing the value and size of the input electrolytic capacitor C_{in} by extending the AC powering time inside one line cycle. The capacitor energy is used only when the AC voltage is below the desired level. The capacitor discharging process is controlled by an auxiliary switch, while the charging is not influenced. This line power extension method can reduce the input capacitor value and size by 25% in the developed prototype at 60 W power. Alternatively, if the same capacitor is used, the DC bus voltage range is reduced as well as the current stress, from which the design of the following DC-DC converter can benefit. It is worth mentioning that the proposed method can be applied to all existing AC-DC solutions, including Flyback, resonant converters, *etc*.

II. Conventional Capacitor Buffering

Fig. 2 shows the waveform of the conventional full bridge rectifier. In the middle, showing in red, is the absolute value of the AC line voltage. On the top, showing is blue, is the voltage on the input capacitor C_{in}, which is also the bus voltage for the following DC-DC converter.

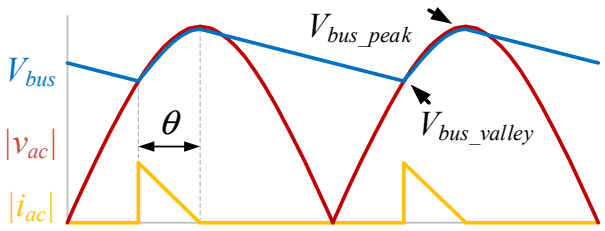


Fig. 2. *Full bridge rectifier conduction waveform*

When the V_{bus} is lower than the line voltage, the capacitor will be charged until the peak line voltage. After that, C_{in} will be discharged to power the load until its voltage is lower than the line again in the next half line cycle.

At given AC voltage, the relationship between V_{bus_peak} and V_{bus_valley} is determined by (1), in which P_o is the output power and Δt is the discharging time of C_{in}.

$$\frac{1}{2}C_{in}\left(V_{bus\_valley}^2 - V_{bus\_peak}^2\right) = P_o \cdot \Delta t \qquad (1)$$

Specifically, Δt can be found in (2), in which f_{line} is the AC line frequency. θ is given in (3).

$$\Delta t = \frac{\pi - \theta}{2\pi f_{line}} \qquad (2)$$

$$\theta = \cos^{-1}\left(\frac{V_{bus\_valley}}{V_{bus\_peak}}\right) \qquad (3)$$

If the capacitor value is high enough so that the voltage drop is neglectable, then the capacitor discharging time is approximately 1/2 f_{line}. Based on this assumption, the DC voltage range on a 100 µF capacitor for 60 W power at different AC voltages is calculated and shown in Fig. 3.

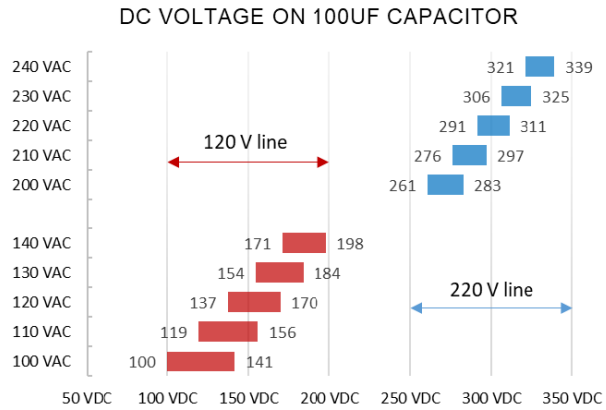


Fig. 3. *DC voltage on 100 µF capacitor for different AC voltages and 60 W load power*

For universal AC input from 100 – 240 VAC, the maximum C_{in} voltage, V_{bus_max}, is well determined, despite the design. V_{bus_max} equals to 340 V, which is the peak voltage at 240 VAC. On the other hand, the minimum C_{in} voltage, V_{bus_min}, is determined by the valley voltage point at 100 VAC. For certain power level, V_{bus_min} varies for different C_{in} values. In this case, with 60 W load and 100 µF of C_{in}, the V_{bus_min} is 100 VDC, at which the converter has the maximum current stresses.

For 100 VAC, if the minimum DC voltage V_{bus_min} is chosen as 100 V, the conduction angle θ (as shown in Fig. 2) is only 45° out of a half line cycle. Equivalently, the input capacitor provides the power for the rest 135° (75% of cycle period). It is noted that the AC line provides the power only before the peak voltage, even though after that the line voltage is still higher than the V_{bus_min}. Thus, if the interval after the peak point till the V_{bus_min} can also be used, then the conduction angle θ can be doubled. Effectively, the capacitor discharging time is reduced. Thus, the required capacitor value can be reduced to achieve the same V_{bus_min}. Alternatively, with the same capacitor value, V_{bus_min} can be increased. Then the voltage gain requirement for the following DC-DC stage will reduce, so does the current stress. This can be further interpreted into either efficiency improvement or size reduction.

III. Operation Principle of the Line Power Extension Method

Fig. 4 shows the line power extension circuit, in which switch S is added to the conventional full bridge rectifier. S should be connected in such way that the current through the body diode will charge the capacitor C_{in}. Thus, despite of the state of S, C_{in} can always be charged when the line voltage is higher than the capacitor voltage. On the other hand, the capacitor can be discharged only when S is turned on.

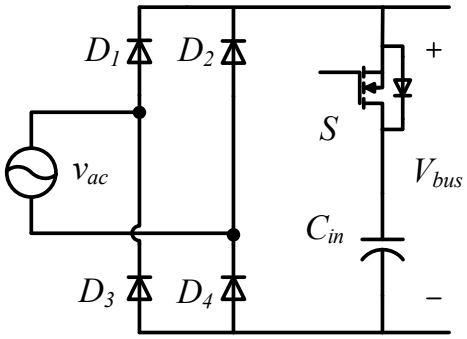


Fig. 4. Line power extension circuit

Fig. 5 shows the key waveforms of the line power extension method. V_{bus} is the output voltage of the line power extension circuit, as well as the input voltage for the next DC-DC stage. $|v_{ac}|$ is the absolute value of the AC input. i_{ac} is the AC input current. G_s is the gate signal of the switch S. The detailed operation in the positive half line cycle is shown in Fig. 6. The negative half cycle has similar operation.

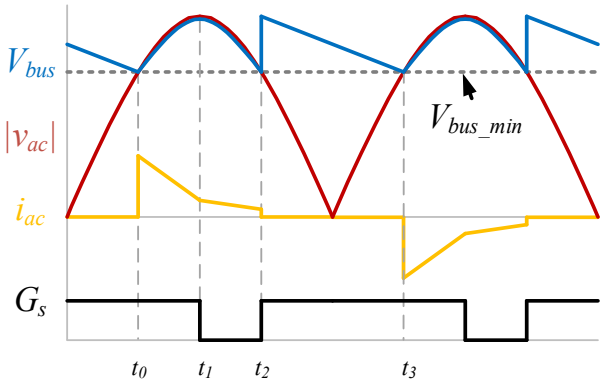


Fig. 5. Key waveform of line power extension

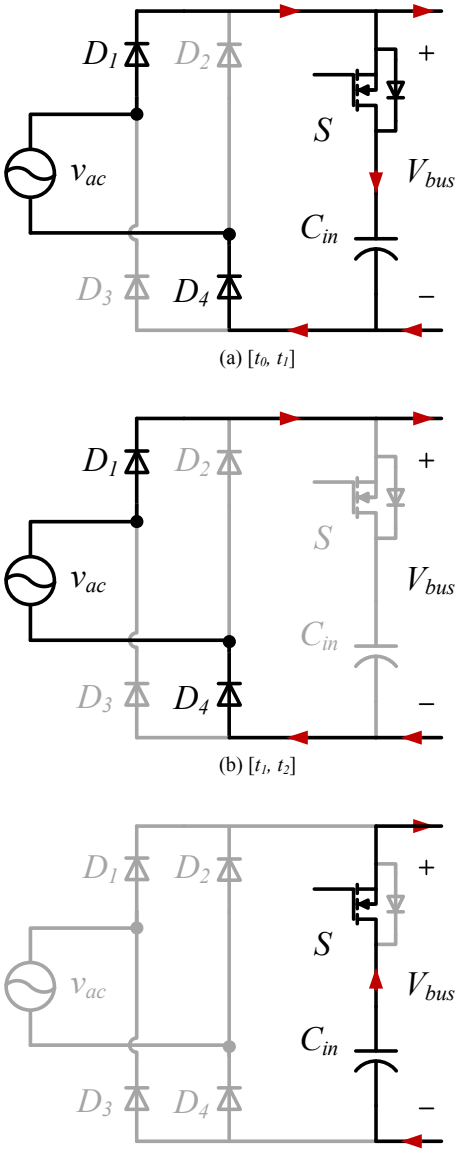


Fig. 6. Detailed operations of the positive half cycle

State a [t_0, t_1]: D_1 and D_4 start to conduct at t_0, at which time v_{ac} equals to V_{bus}. From t_0 to t_1, the capacitor voltage will increase with v_{ac}. During this process, S is preferred to be turned on, in order to reduce the conduction loss. In ideal case, S should be turned off at t_1, at which the capacitor voltage reaches the peak value. However, in practice, S can be turned off between t_0 and t_1 to avoid fault operation. The capacitor can still be charged through body diode to the peak line voltage.

State b [t_1, t_2]: As S turns off at t_1, the capacitor is disconnected from the load, thus the capacitor voltage will remain as the peak line voltage. The load is powered by the AC line directly during t_1 to t_2, and the AC current equals to the AC voltage over the load resistor. Due to this extended conduction time of the line power, i_{ac} is lower than the conventional full bridge. During t_1 to t_2, the body diode of S is reverse-biased. The peak voltage stress on S is reached at t_2, whose value equals to V_{bus_max} – V_{bus_min}. For the most part, the voltage stress is below 100 V.

State c [t_2, t_3]: After t_2, v_{ac} reduces below the designed V_{bus_min}. S is turned on at t_2, so that the capacitor energy is used. As the capacitor voltage is maintained at the peak line voltage, D_1 and D_4 will be reverse-biased after t_2. The capacitor voltage will reduce until equal to v_{ac}. In this case, the capacitor value is selected such that the minimum capacitor voltage at t_3 is equal to the line voltage at t_2, both at V_{bus_min}.

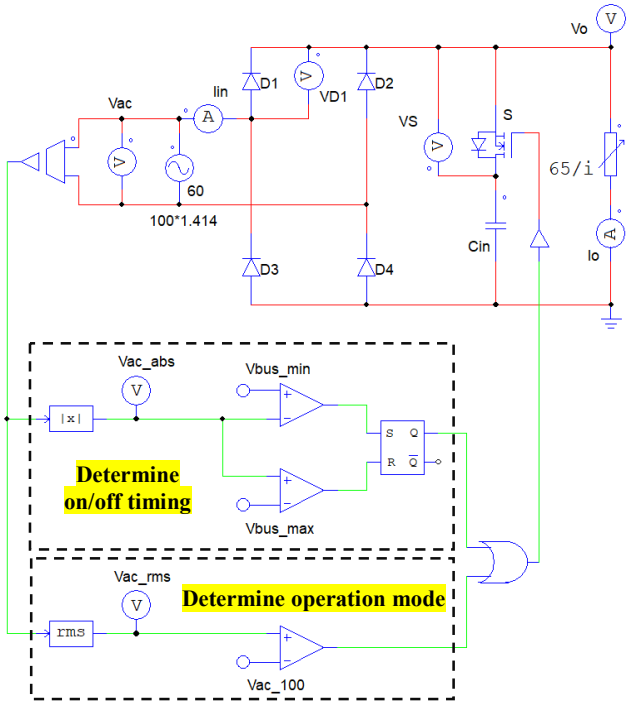


Fig. 7. Circuit diagram and control logic

IV. CONTROL LOGIC

The circuit diagram and control logic are shown in Fig. 7. The lower box shown in Fig. 7 is used to determine the operation mode of the control circuit, *i.e.* if line power extension is needed. The line power extension control only takes effect when the AC voltage is low, *e.g.* 100 VAC. For normal operation at 120 VAC, the bus voltage should always be higher than the designed V_{bus_min}. Thus, there is no need to perform the control. The switch should remain as on, and the circuit is equivalent to the conventional full bridge rectifier.

The upper box is used to determine the on/off timing of the switch *S*. In ideal case, *S* should be turned off at the line peak, after which the line will power the load directly. The turn on timing of *S* is when the line voltage reduces to the designed V_{bus_min}. Since *S* is turned on lower voltage level and turned off at high level, there is no conflict on the timing, leading the entire control very straightforward.

V. PERFORMANCE COMPARISON

With the AC line provides more power, the capacitor does not need to store as much energy as that in the full bridge case. Thus, the capacitor value can be reduced while achieve same bus voltage range. Fig. 8 shows the simulation results of the required capacitance for both the line power extension method and conventional full bridge for different V_{bus_min} designs and 60 W load.

If the V_{bus_min} is designed at 50 V, then 37 µF capacitance should be used for full bridge, while only 15 µF is needed with the line power extension. Thus, 59% of capacitor reduction can be achieved for 50 V design. The capacitor reduction ratio will reduce with the V_{bus_min} increases, as the AC power conduction angle is reduced. In practice, a typical V_{bus_min} design is 90 V-100 V, at which 1/3 of capacitance can be saved with the line extension method.

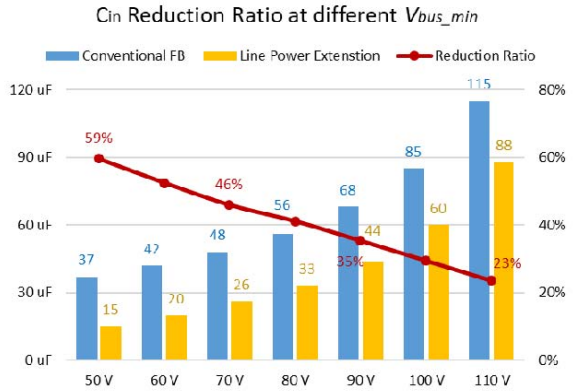


Fig. 8. Required C_{in} for different V_{bus_min} for 100 VAC

If the same capacitance is used, then the V_{bus_min} can be increased to relieve the wide gain requirement for the following stage. Fig. 9 shows the comparison of the minimum bus voltage between the conventional full bridge and the line extension method for different C_{in} values. In some extreme case with a 39 µF capacitor used, then the V_{bus_min} for the full bridge is only 55 V, while that for the line power extension method is 86 V. Referring to the same V_{bus_max} of 340 V, the normalized voltage gain requirement is reduced from 6.2 to 4. In other words, the gain requirement reduces to only 64% of that in the full bridge. With the applied C_{in} increases, the conduction angle reduces, thus the line power shows less significance.

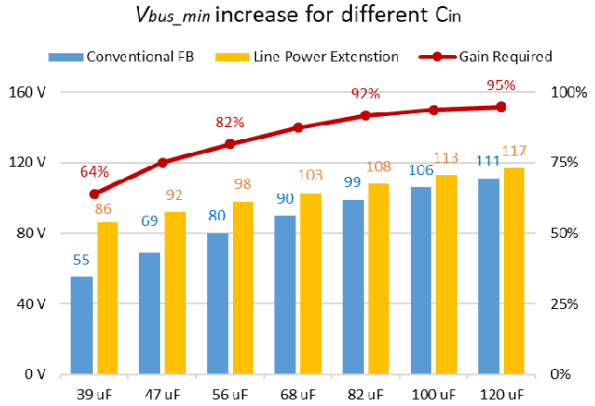


Fig. 9. Achieved V_{bus_min} at given C_{in} for 100 VAC

In a practical case, if an 82 µF capacitor is used, then the V_{bus_min} can be increased from 99 V in conventional full bridge to 108 V with the line power extension circuit, which is ~10% of improvement. In some topologies, *e.g.* series resonant converter, this 10% voltage improvement indicates the same amount of current stress reduction. Then, the conduction loss can be reduced to only 81% (= 0.9^2) of the that in the full bridge case.

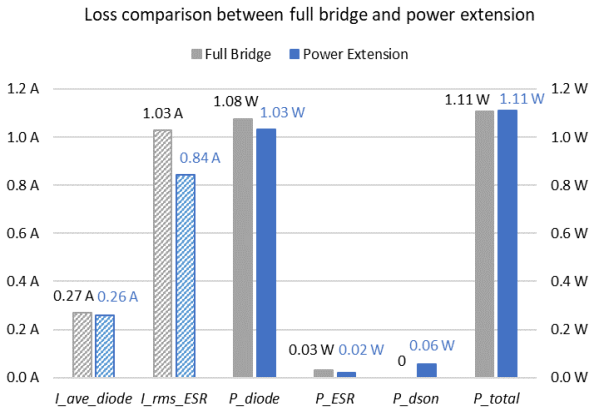


Fig. 10. Current and loss comparison of full bridge rectifier and the line power extension method

Besides the significant current reduction for the following DC-DC converter, the current stress in the input rectifiers are also slightly reduced with the voltage improvement. Fig. 10 shows the current stress and loss comparison of full bridge rectifier and the line power extension method. The diode loss is calculated based on 0.95 V forward voltage drop (Part No. LB6S), while the MOSFET conduction loss P_{dson} is calculated based on R_{dson} of 85 mOhms (Part No. STF43N60DM2). It can be observed that the diode bridge has significantly higher loss as compared to the additional switch. The extra loss created by the additional switch can be compensated by the reduced current stress in diode bridges, so that the total loss in this two configuration are same in this case. If the losses in the EMI filter is also considered, then the line extension circuit actually help reduced the total loss.

VI. Experiment Results

A 60 W prototype was built to verified the feasibility and demonstrate the advantages of the proposed line power extension circuit. The parameter design and the specifications are shown in Table I. Total 60 µF (56 µF electrolytic + 4.7 µF ceramic) capacitance is needed to maintain the V_{bus_min} as 100 VDC for 100 VAC. As comparison, 85 µF (82 µF electrolytic + 3.3 µF ceramic) should be used to achieve same input voltage range.

Fig. 11 shows the size comparison of 56 µF and 82 µF electrolytic capacitors from United Chemi-Con PAG series. Both capacitor has the same diameter of 16 *mm*. The length of the 56 µF capacitor is 30 *mm*, while that of the 82 µF capacitor is 40 *mm*. Thus, a 25% size reduction is achieved with the line power extension circuit.

Table I. Specifications of Line Power Extension Method

Input AC voltage	100VAC – 240VAC
Operation of Line Power Extension	100VAC
Operation as Full Bridge	110VAC – 240VAC
Output Power	60 W
Input capacitor C_{in}	56 µF (electrolytic) + 4.7 µF (ceramic)
Minimum Bus Voltage V_{bus_min}	100 VDC
Auxiliary MOSFET	STF43N60DM2 (85mOhms)
Diode Bridges	LB6S (0.95V)
Controller	dsPIC33FJ06GS101A
Auxiliary MOSFET Driver	PC817

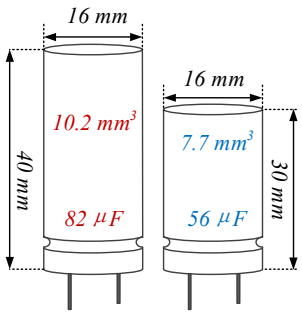
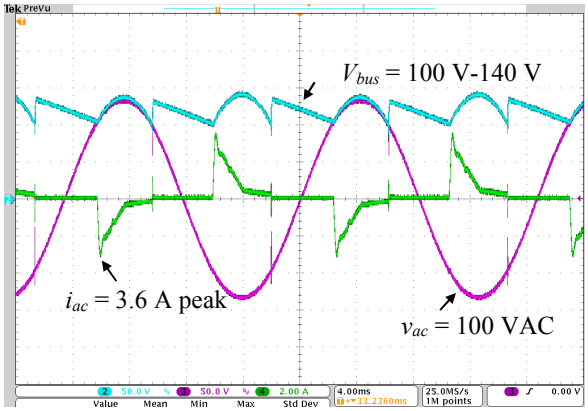


Fig. 11. Capacitor size comparison of full bridge and line power extension method

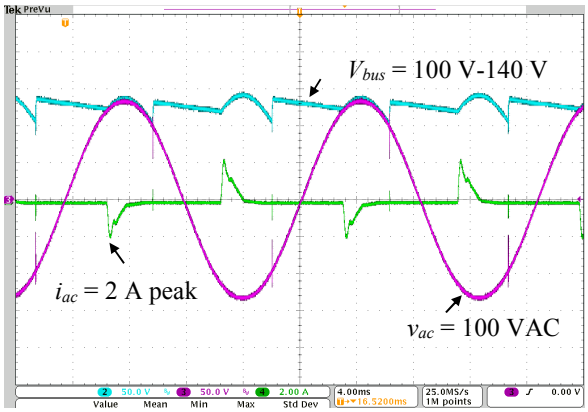
Fig. 12 shows the waveform under 100 VAC input and 60 W load power. Channel 2 shown in blue is the bus voltage. The minimum value is controlled at 100 V. For 60 W load, the peak AC current stress is 3.6 A.



Ch2: V_{bus} (50 V/div); Ch3: V_{ac} (50 V/div); Ch4: I_{ac} (2 A/div)

Fig. 12. Waveform for 100 VAC and 60 W load

Fig. 13 shows the waveform under 100 VAC input and 30 W load power. Still, the minimum bus voltage is controlled at 100 V. With 30 W load, the capacitor voltage variation is smaller.



Ch2: V_{bus} (50 V/div); Ch3: V_{ac} (50 V/div); Ch4: I_{ac} (2 A/div)

Fig. 13. Waveform for 100 VAC and 30 W load

VII. CONCLUSION

In this paper, an AC power extension method is proposed to reduce the value and size of the input capacitor in AC-DC applications. This method can be applied to all existing DC topologies, including Flyback and resonant converters. An auxiliary switch is added to the conventional full bridge rectifier to control the capacitor discharge timing. With this method, the load draws more power from the AC line directly when the voltage is above the desired value. Thus, the capacitor provides less power as compared to the full bridge, and the required capacitance is reduced. If the same capacitance is used, the DC bus voltage will be increased, which simplifies the converter design and reduces the current stress. A 60 W prototype is built, and it verified the feasibility and advantages. In the prototype, the electrolytic capacitor value reduces from 82 μF to 56 μF, which is 30% reduction in capacitance and 25% reduction in size.

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